

FIG.

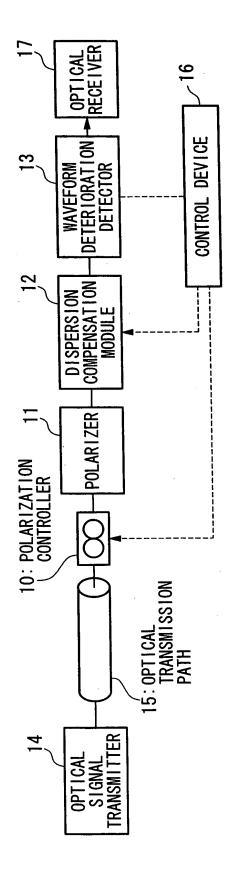
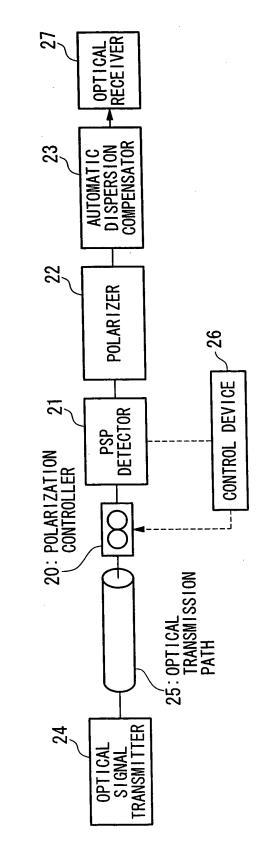
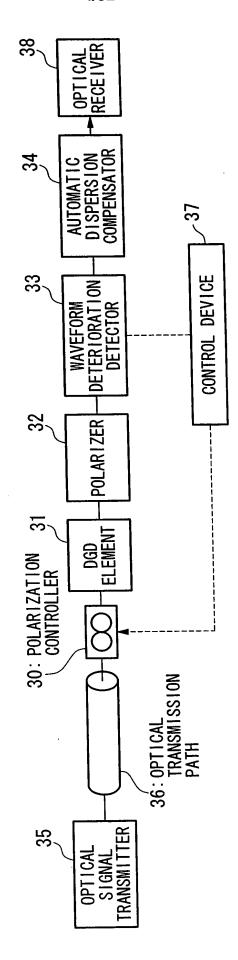
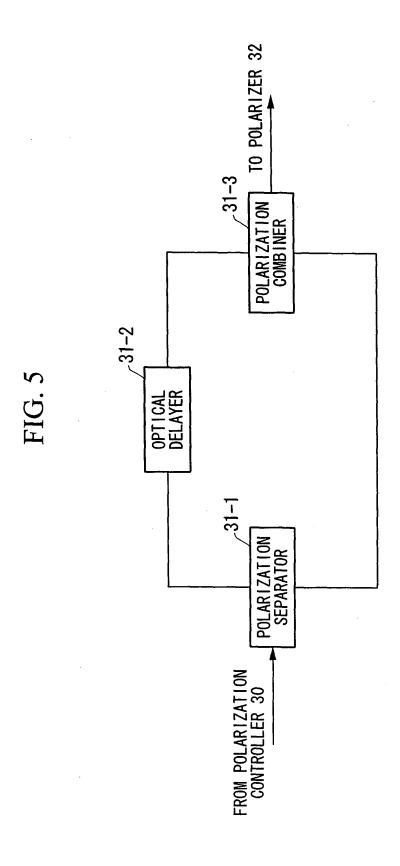


FIG. 2

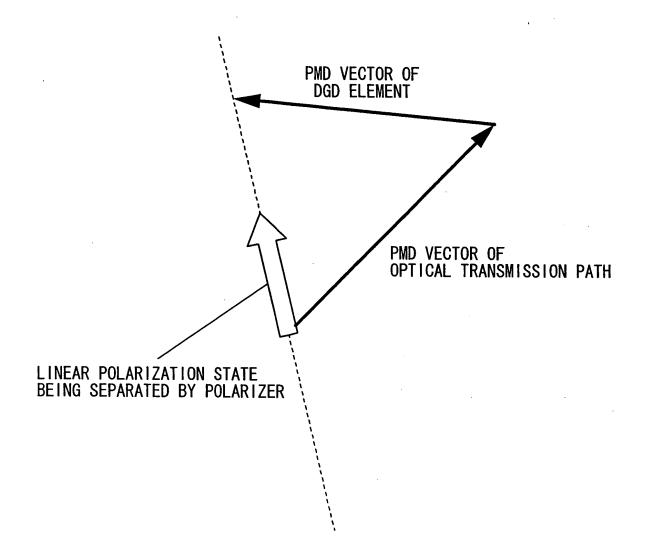


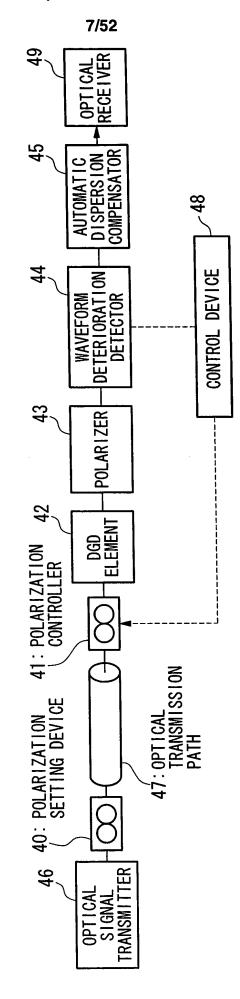
4/52

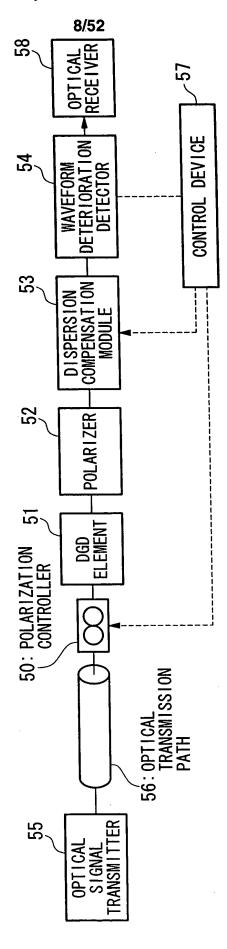




6/52 FIG. 6







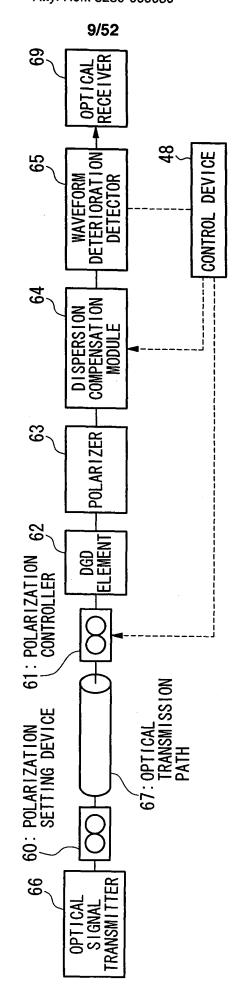
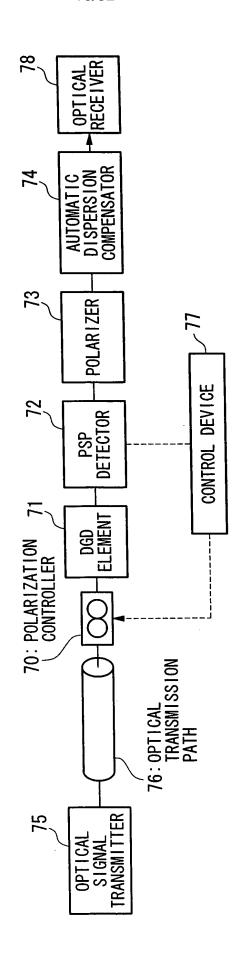


FIG 0

10/52



11/52

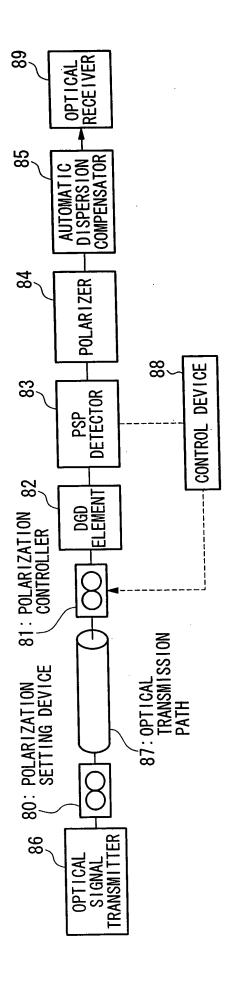


FIG. 11

12/52

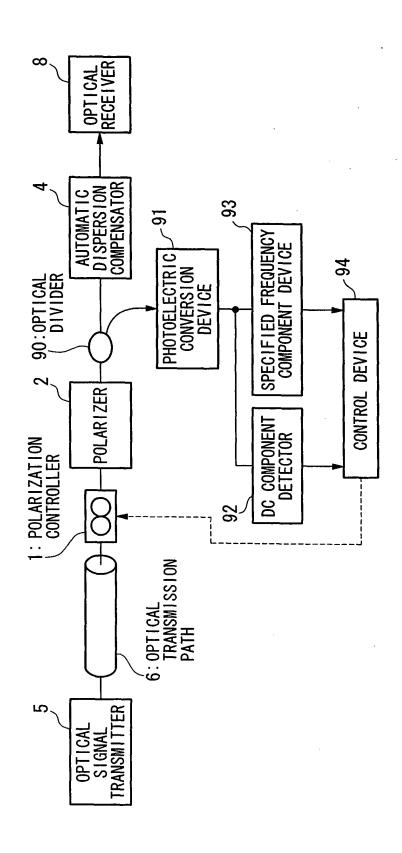
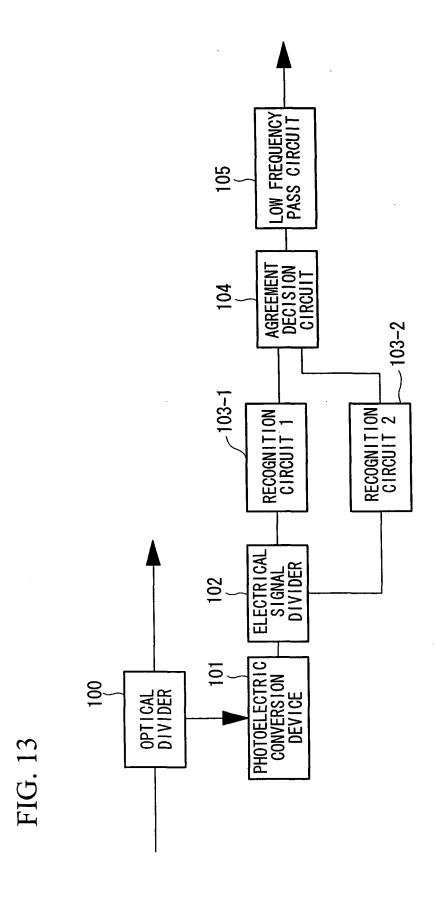
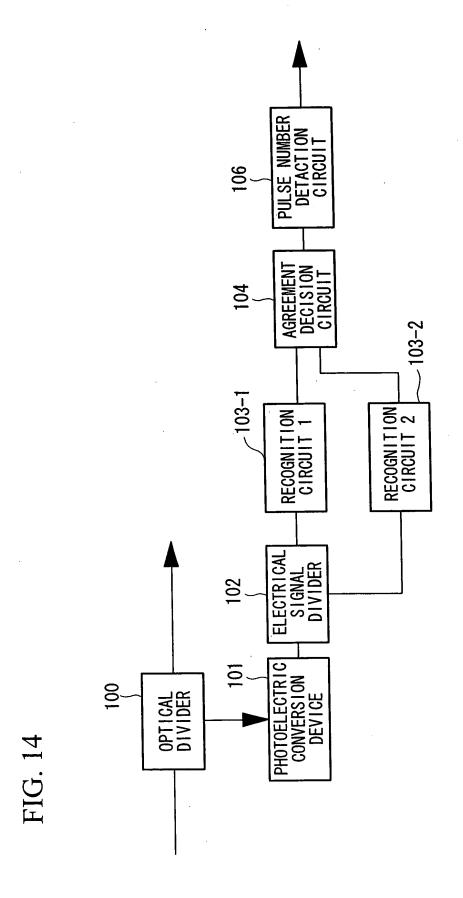


FIG. 12

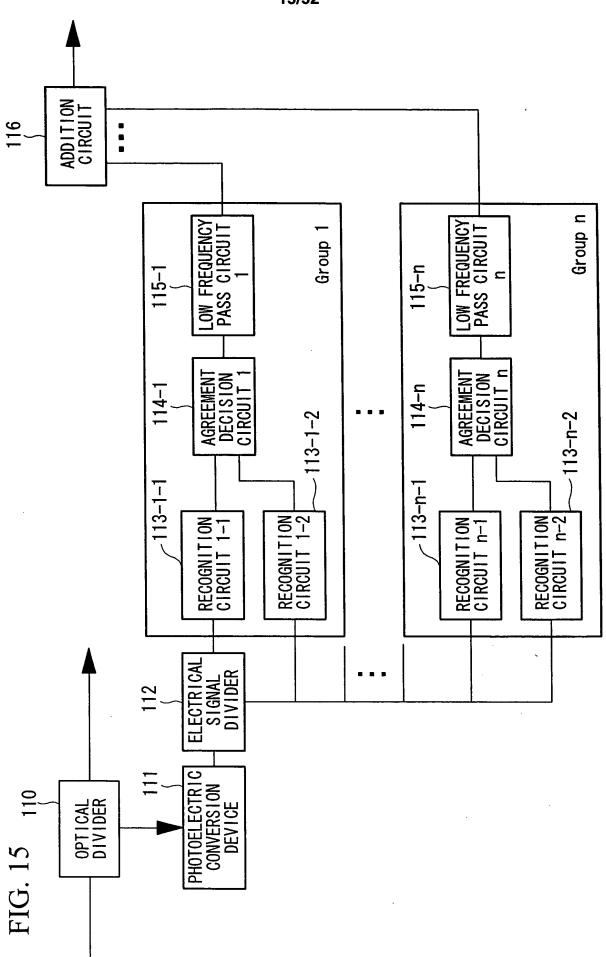
13/52



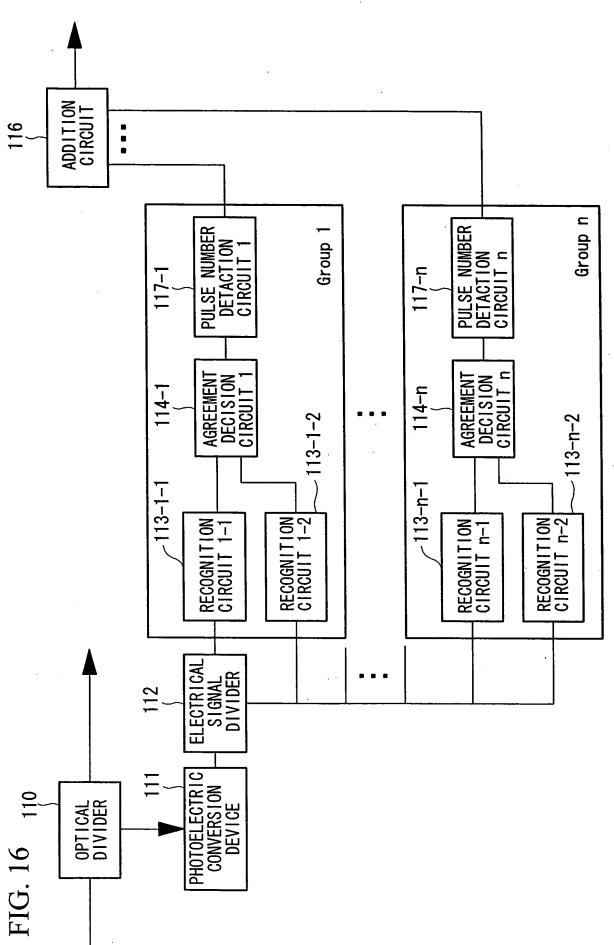
14/52



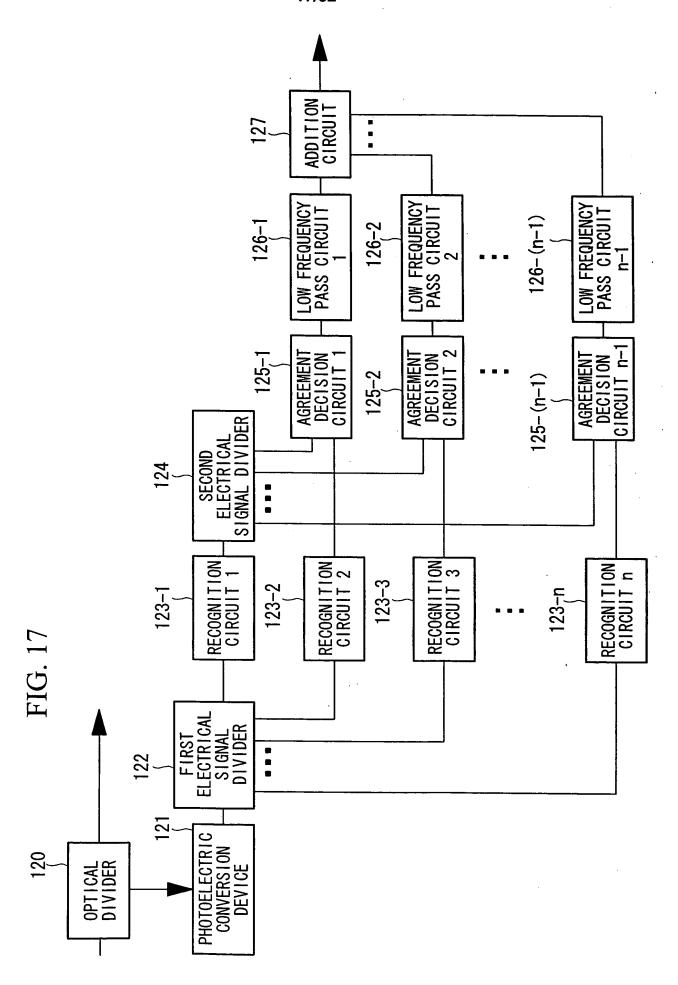
15/52



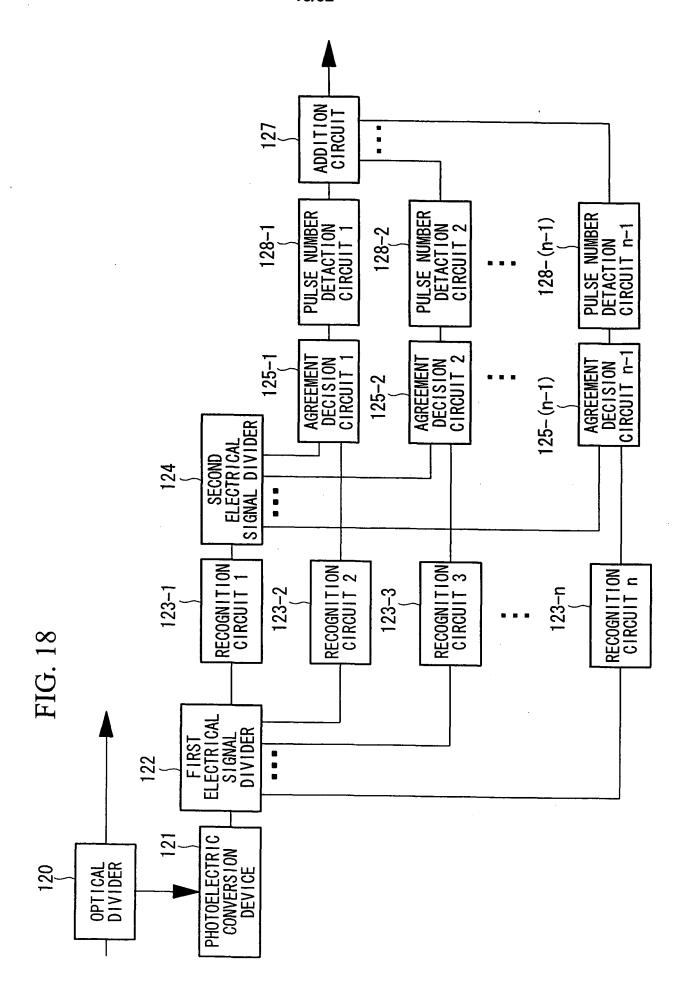
16/52

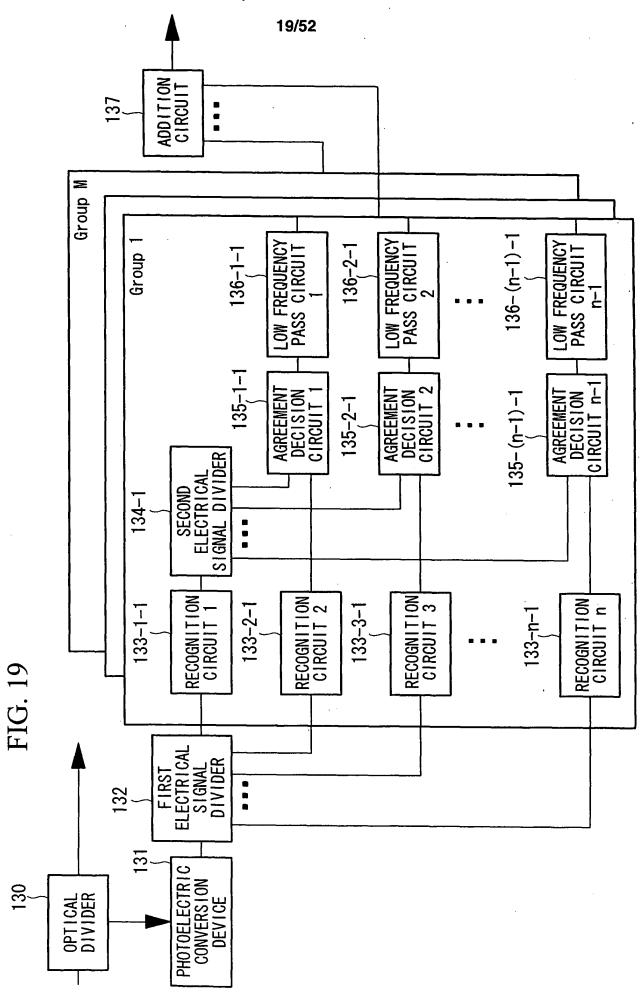


17/52



18/52





Inventor(s): Yoshiaki Kisaka et al. Atty. Ref.: 5259-000030 20/52 ADD I TION CIRCUIT 37 Group PULSE NUMBER DETACTION CIRCUIT 1 PULSE NUMBER DETACTION Group 1 138,-2-1 PULSE NUMBER DETACTION CIRCUIT 2 AGREEMENT DECISION CIRCUIT 2 AGREEMENT DECISION CIRCUIT 1 AGREEMENT DECISION CIRCUIT n-1 |35- (n-1) -1 135-2-1 SECOND ELECTRICAL SIGNAL DIVIDER 134 - 1-RECOGNITION CIRCUIT 1 RECOGNITION CIRCUIT 2 RECOGNITION CIRCUIT 3 RECOGNITION CIRCUIT n 133-2-1 133-3-1 133-1-1 133-n-1 FIRST ELECTRICAL SIGNAL DIVIDER -132 131 PHOTOELECTRIC CONVERSION DEVICE OPT I CAL DIVIDER

FIG. 20

130

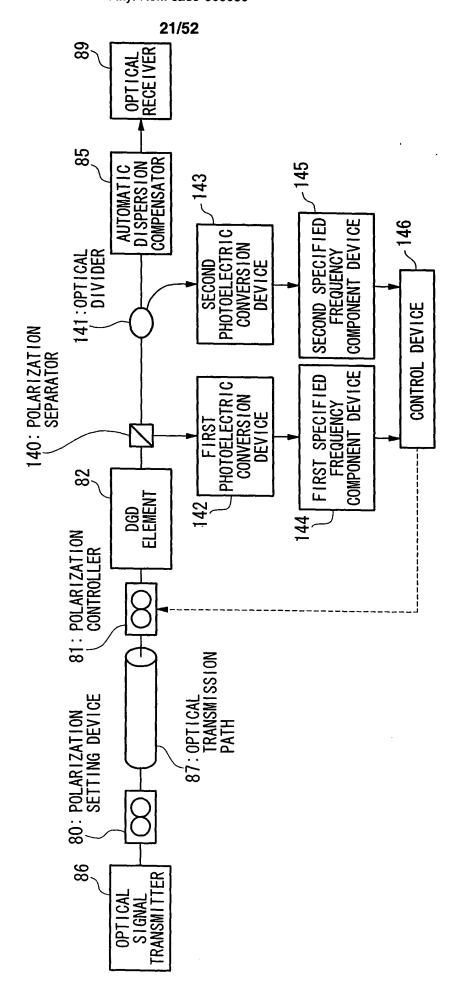
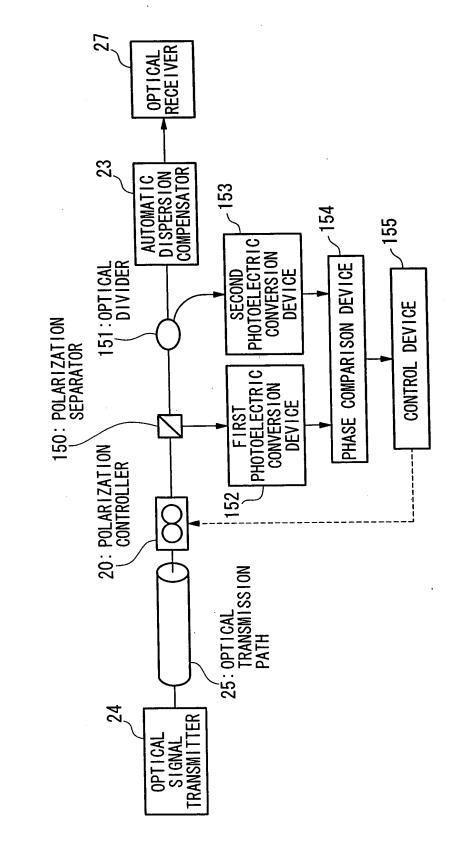
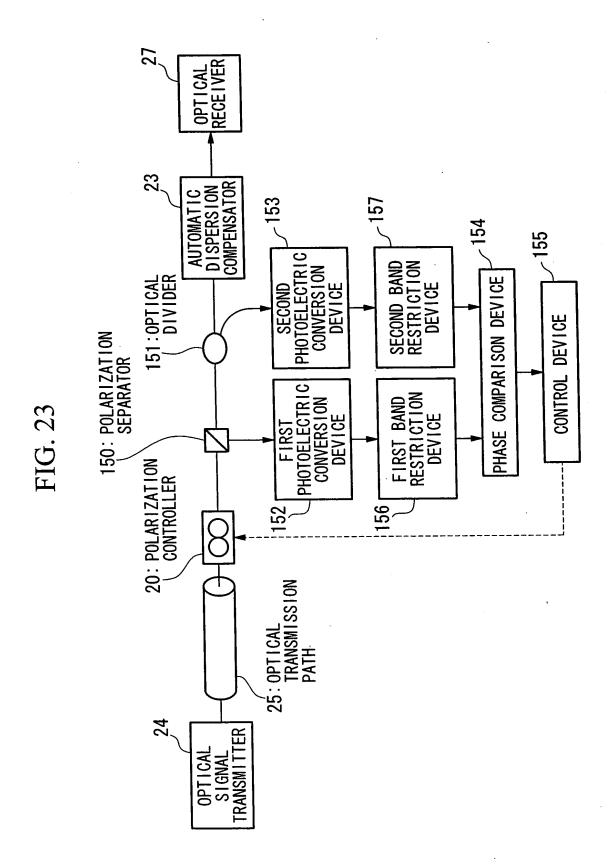


FIG. 2

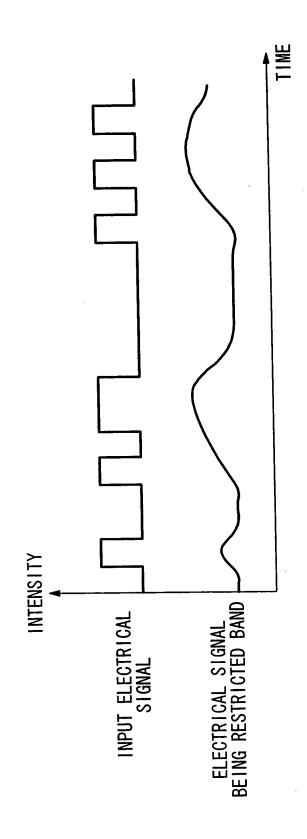
22/52



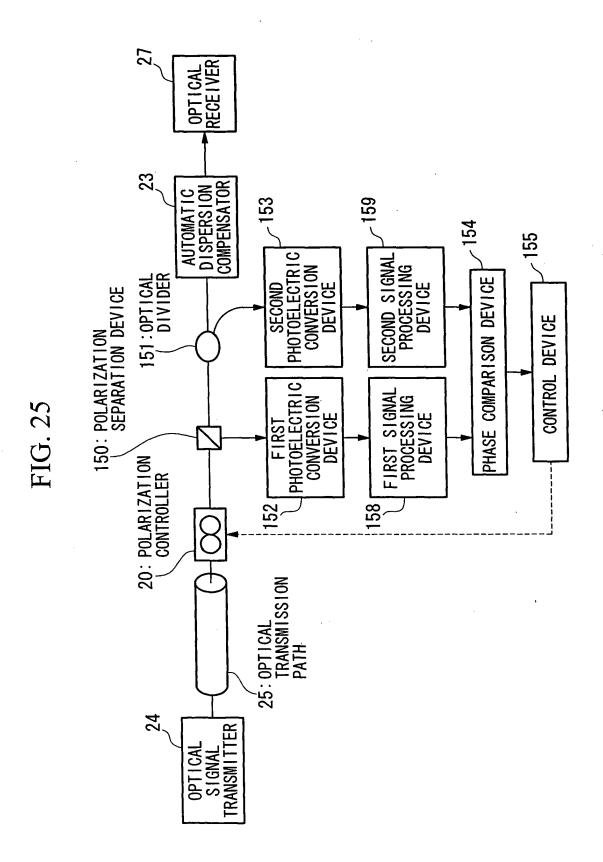
23/52



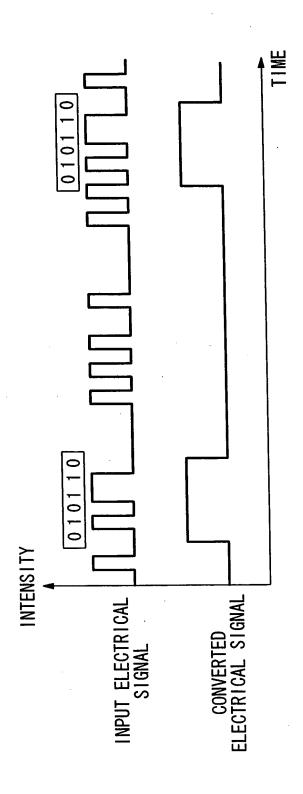
24/52



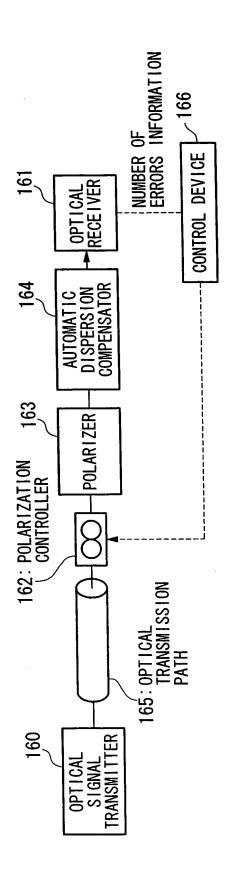
25/52



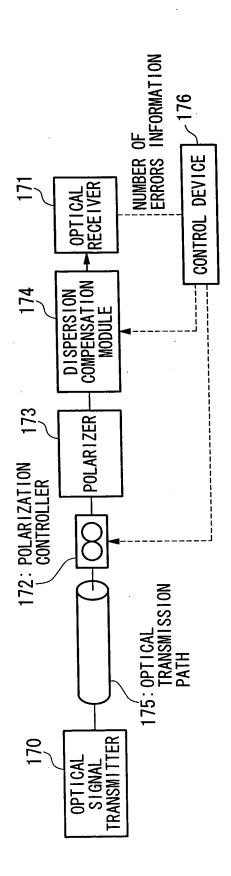
26/52



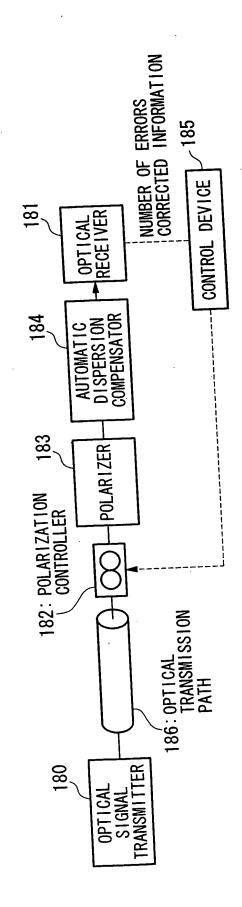
27/52



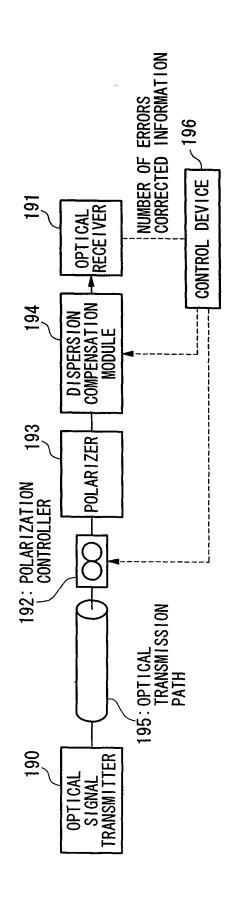
28/52



29/52



30/52



31/52

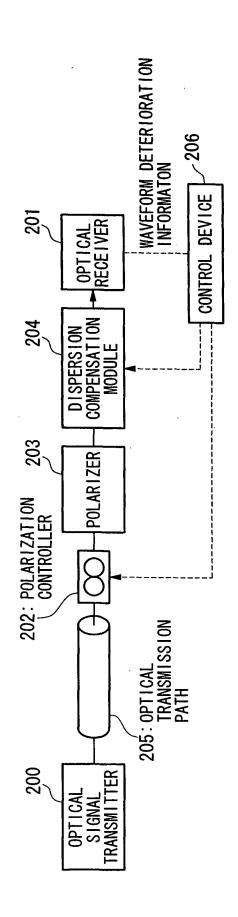


FIG 31

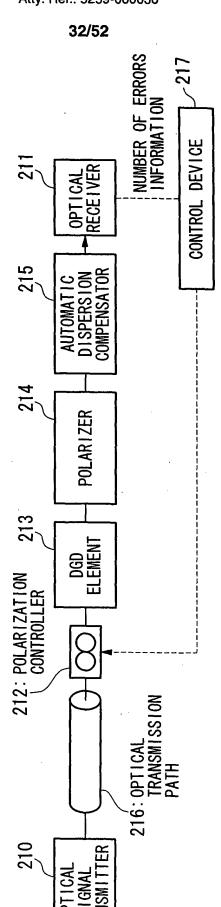
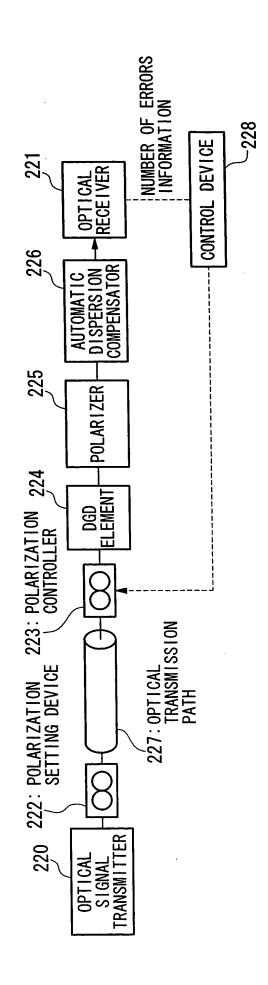
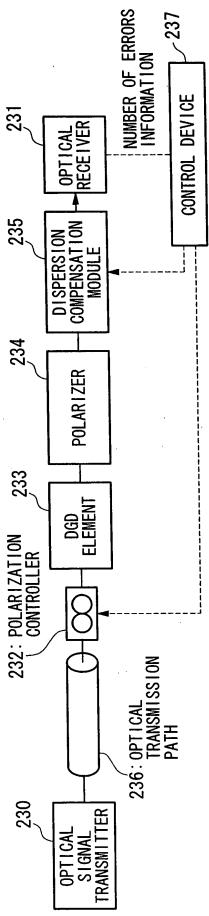


FIG. 32

33/52







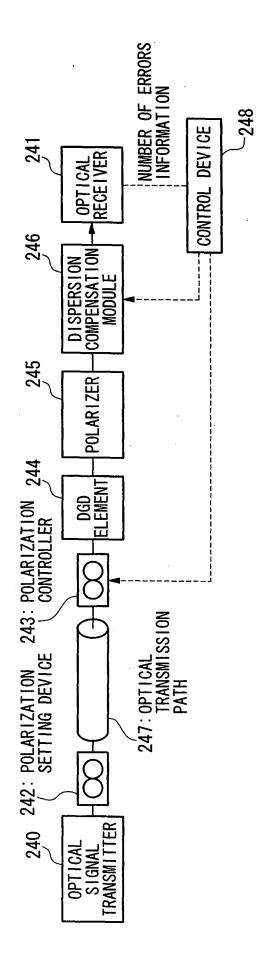


FIG 34

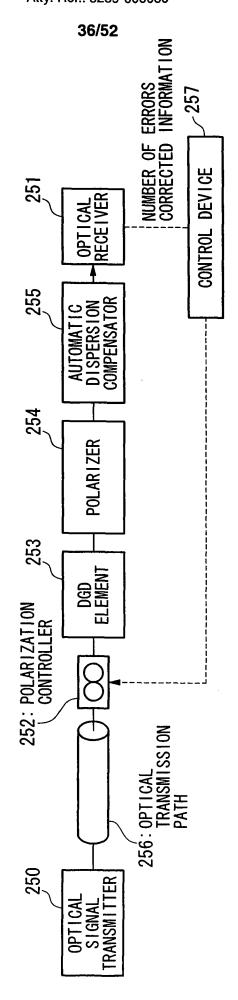


FIG. 36

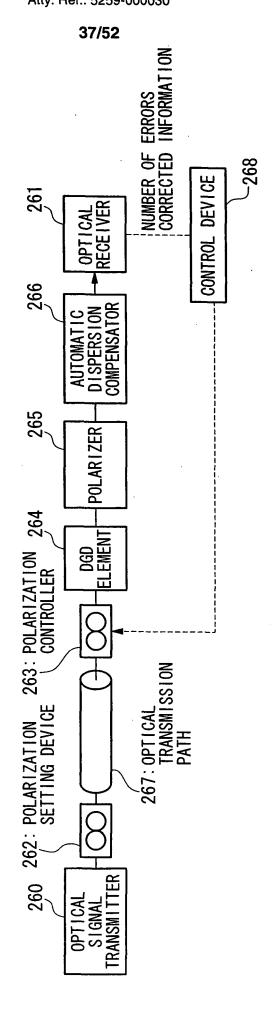


FIG 37

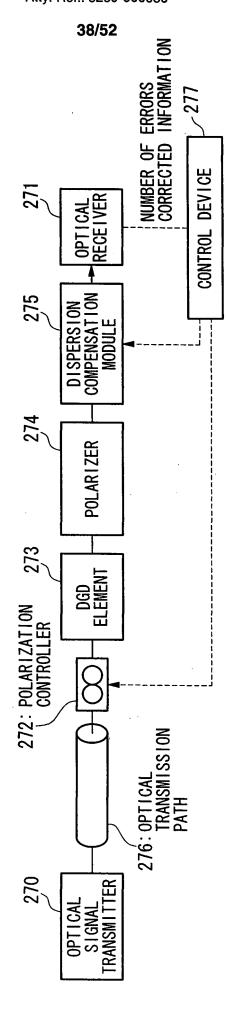


FIG. 38

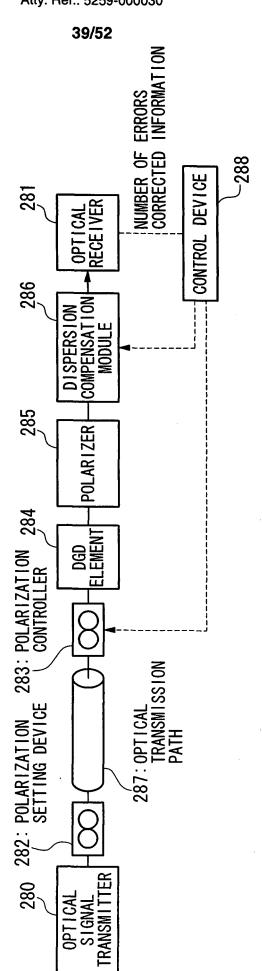


FIG 39

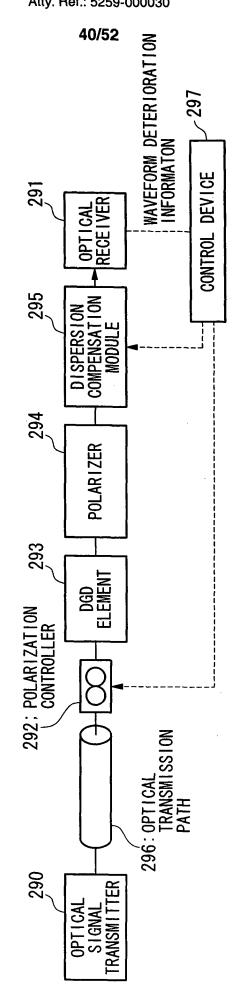


FIG 40

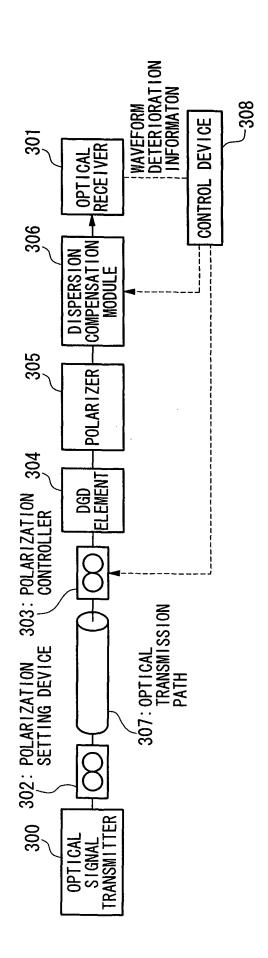
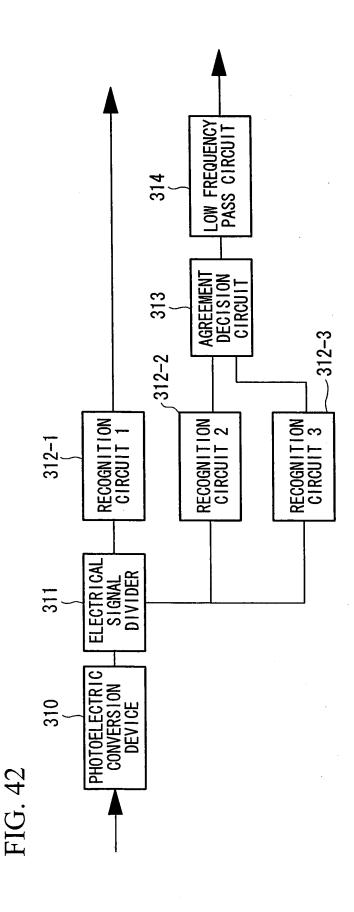


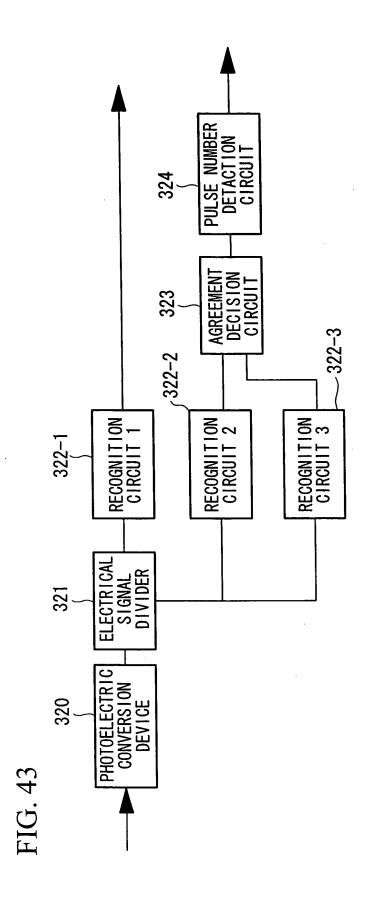
FIG 41

42/52

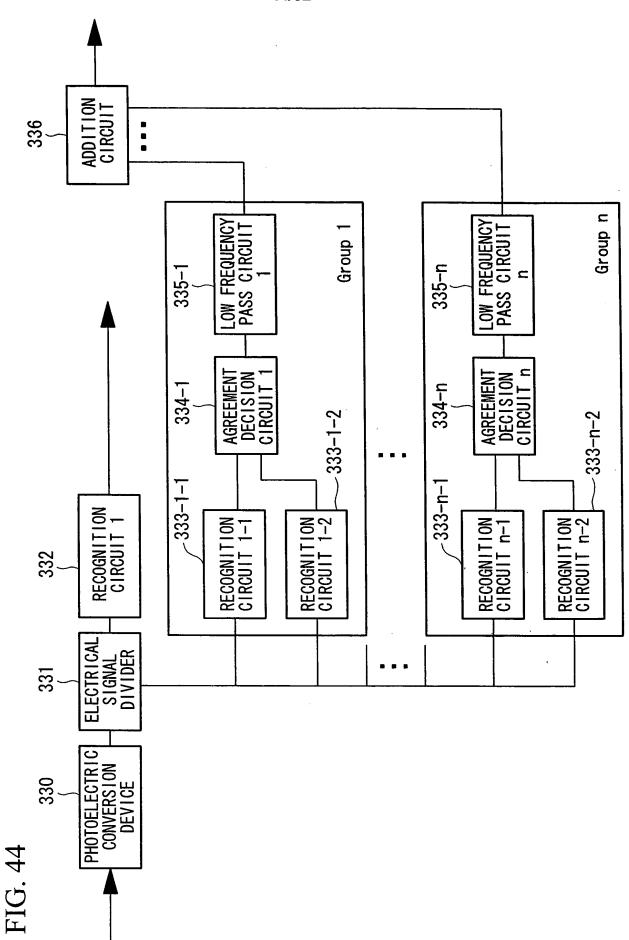


POLARIZATION MODE DISPENSION COMPENSATION DEVICE

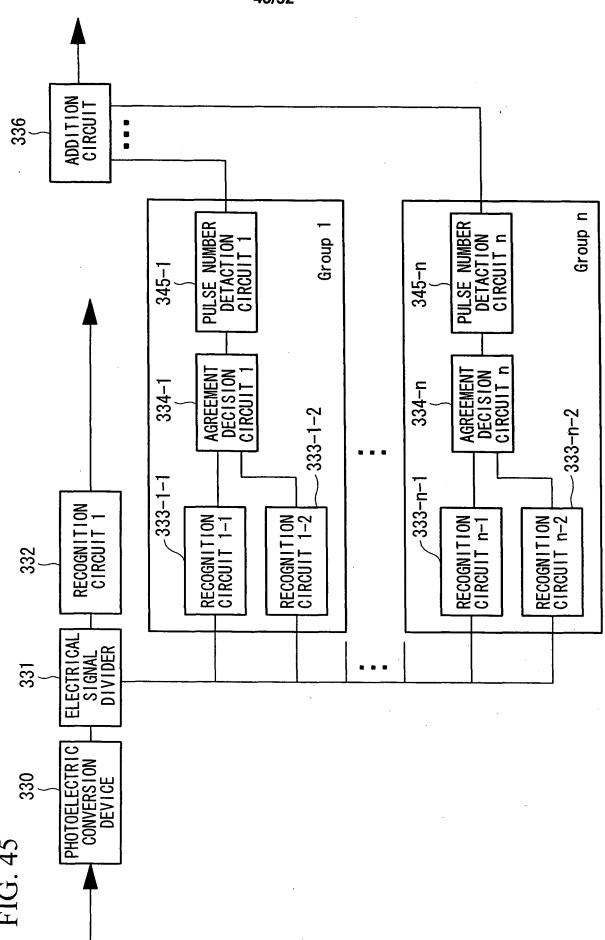
43/52

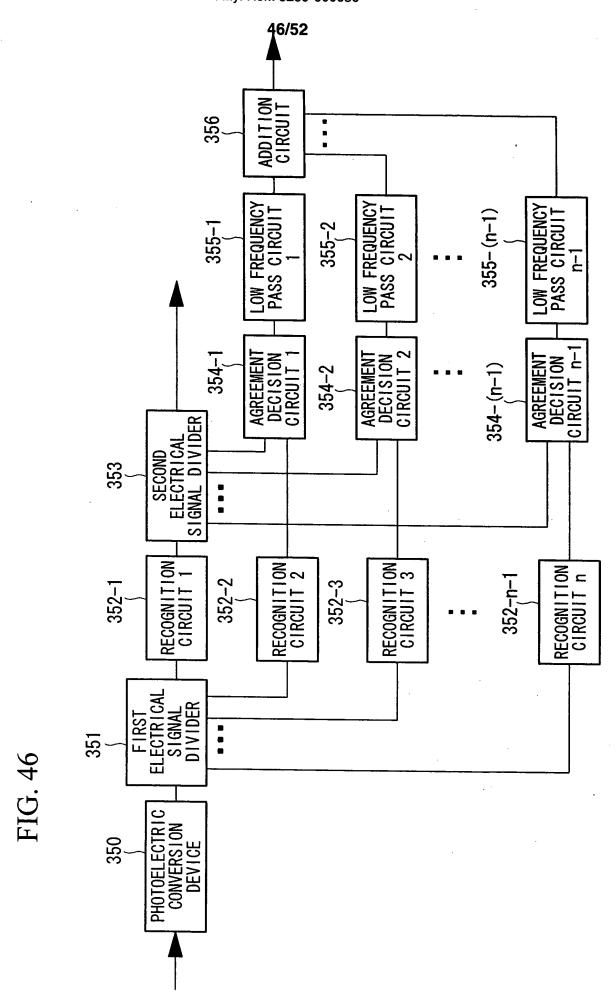


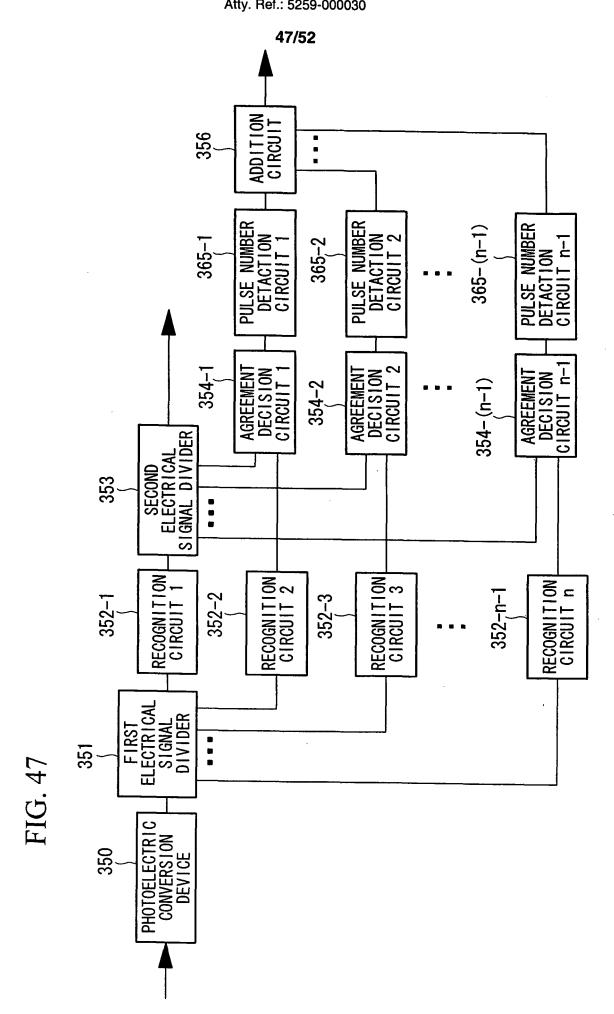




45/52







48/52 FIG. 48

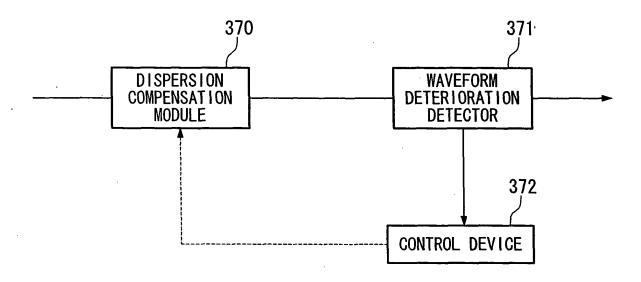
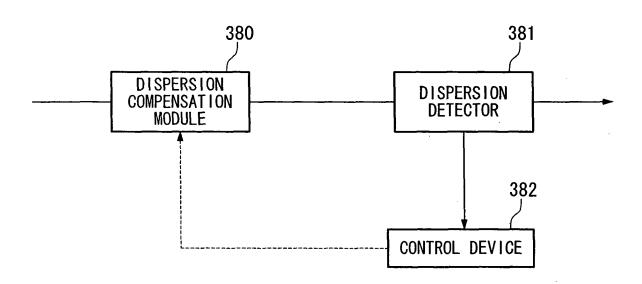
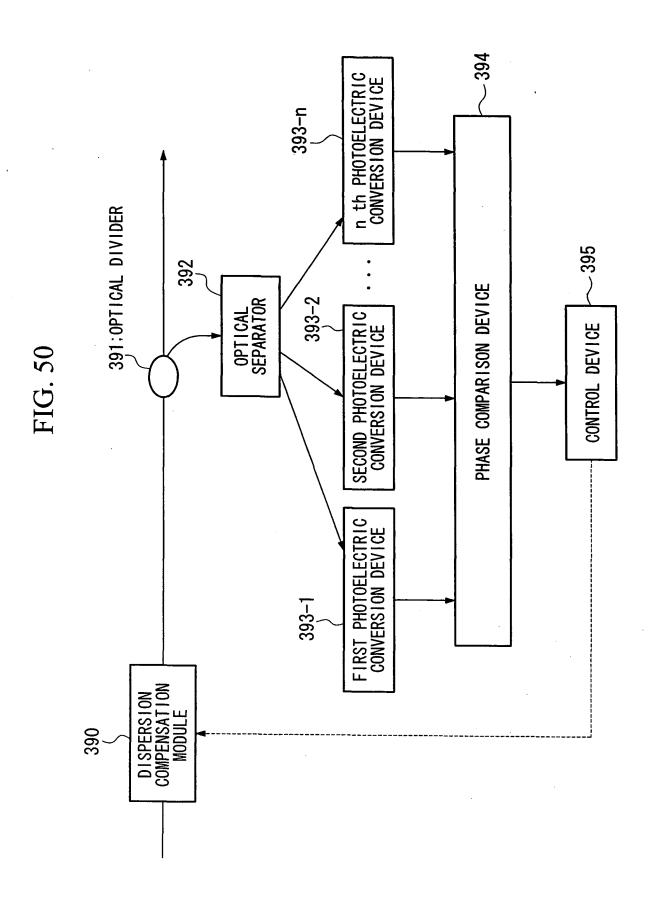


FIG. 49



49/52



50/52

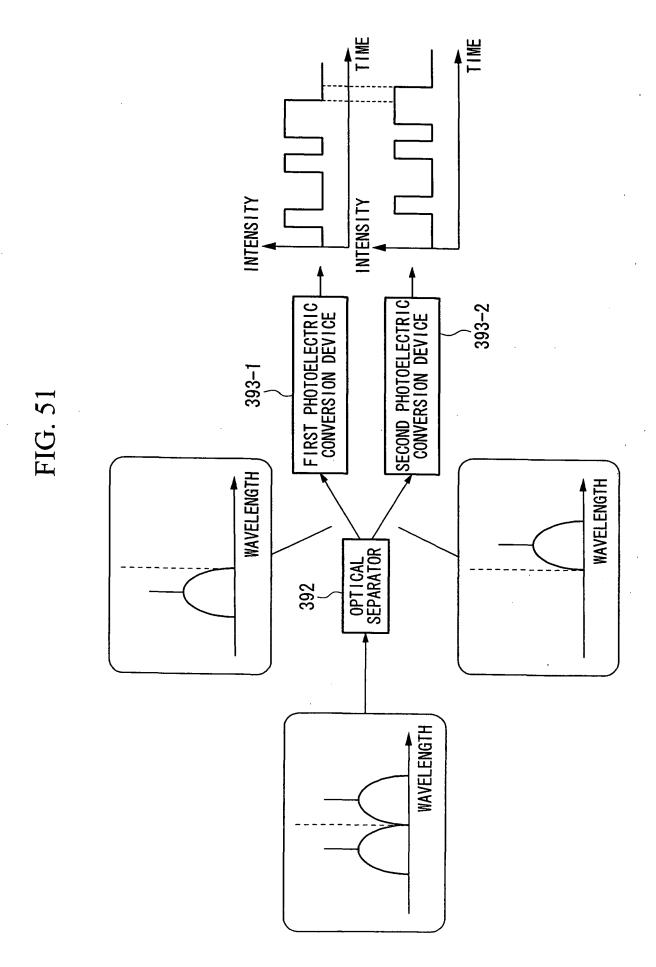


FIG. 52

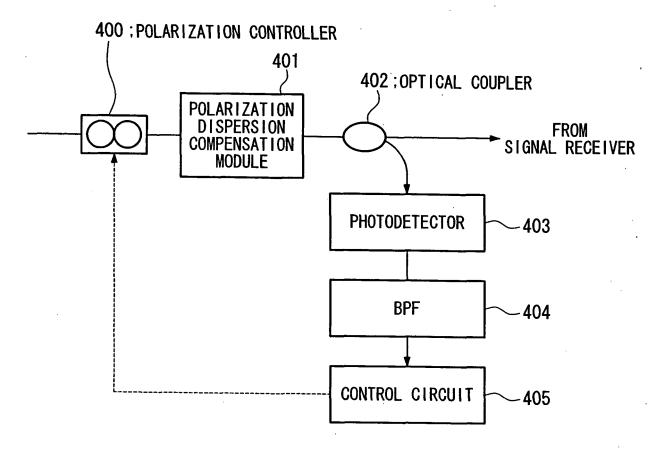
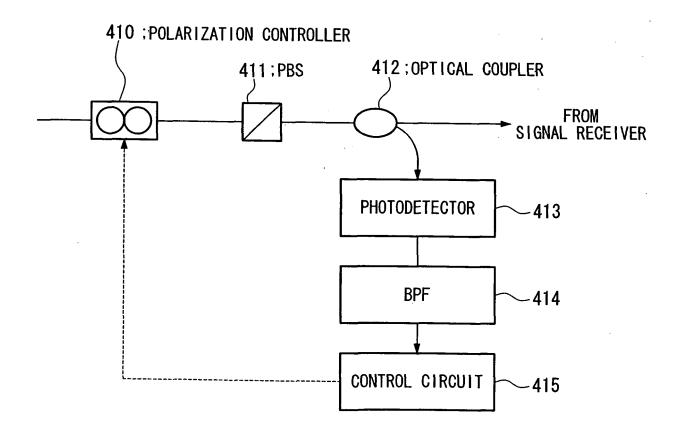


FIG. 53



52/52 FIG. 54

